AMENDMENTS TO THE CLAIMS

This listing of claims replaces all previous versions and listings of claims in this application.

Claim Listing:

Claims 1-2: (Canceled).

3. (Currently amended) A semiconductor integrated circuit, comprising on the same chip:

a plurality of circuit blocks composed by the CMOS process, which have ON/OFF functions of ~~the~~ a power source;

a control circuit to control the ON/OFF functions of the power source of said plurality of circuit blocks; and

analog control lines connected between said plurality of circuit blocks and said control circuit;

wherein, when the power source of a certain circuit block is turned ON by said control unit, another circuit block is controlled so as to not be in an ON state simultaneously with said certain circuit block,

wherein said analog control lines to said another circuit block are wired ~~outside the layout of said plurality of circuit blocks; or on the~~ on a layout of a said certain circuit block~~, analog control lines to another circuit block are wired;~~

~~when the power source of said certain circuit block is turned ON by said control circuit, said another circuit block is not controlled in a state of being ON simultaneously therewith~~.

4. (Original) A semiconductor integrated circuit composed by CMOS structure, comprising:

an analog circuit with feedback loop;

wherein an analog signal line for said feedback is wired outside the layout of said analog circuit.

5. (New) A semiconductor integrated circuit, comprising:

a single chip;

first and second CMOS circuit blocks arranged on the single chip;

a control circuit that at least controls ON/OFF functions of each of the first and second CMOS circuit blocks; and

analog control lines connected between said each of the first and second CMOS circuit blocks and said control circuit;

wherein said analog control lines are arranged over a layout of at least one of the first and second CMOS circuit blocks,

wherein said control circuit controls analog processes in each of the first and second CMOS circuit blocks in a manner that suppresses mutual interference between the first CMOS circuit block and the second CMOS circuit block.

6. (New) The semiconductor integrated circuit of claim 5, wherein the control circuit is located on the single chip.

7. (New) The semiconductor integrated circuit of claim 5, wherein the control circuit controls power applied to each of the first and second CMOS circuit blocks in a manner that ensures that when the first CMOS circuit block is powered, the second CMOS circuit block remains unpowered.